

FIG. 1

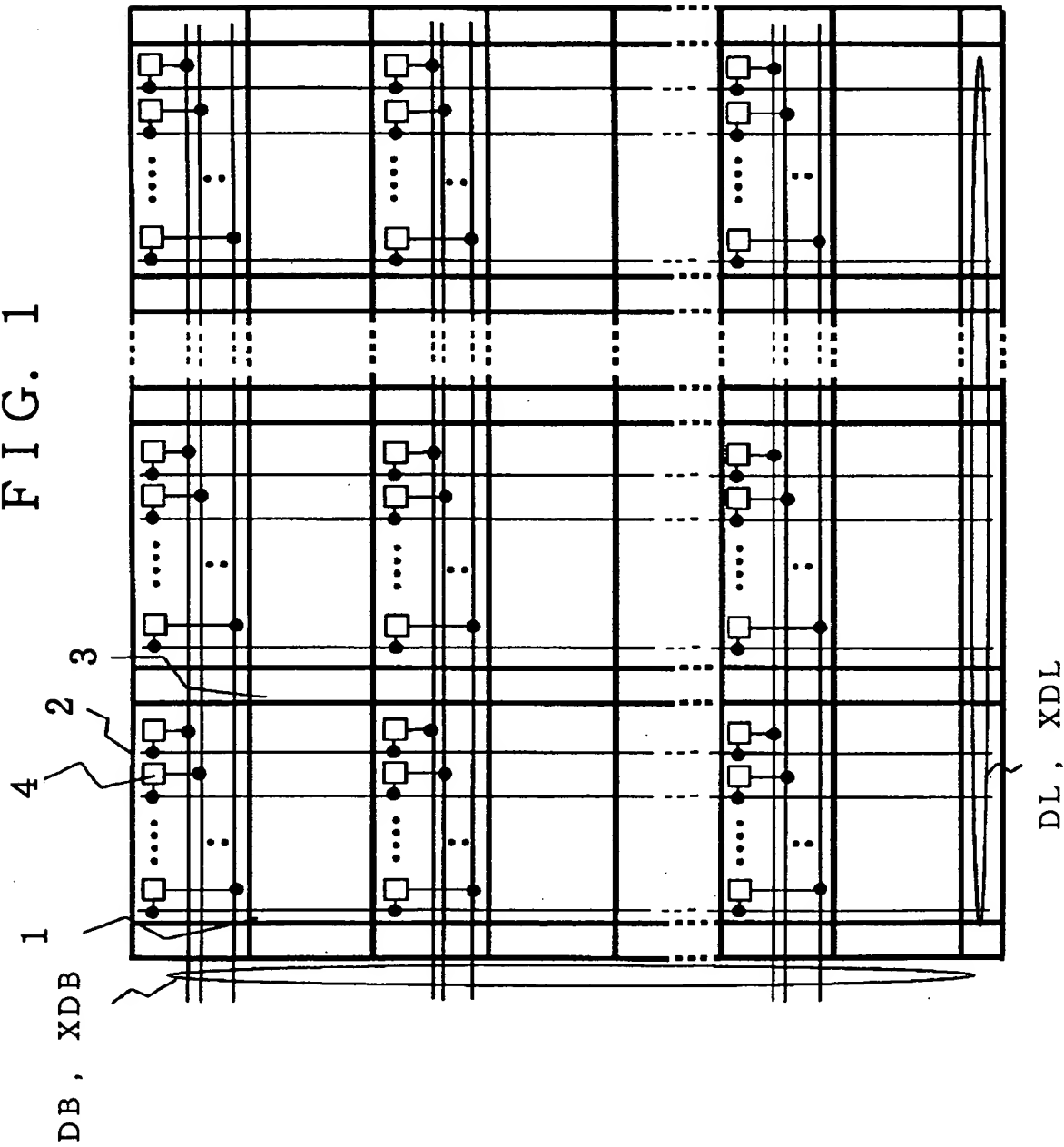




FIG. 3

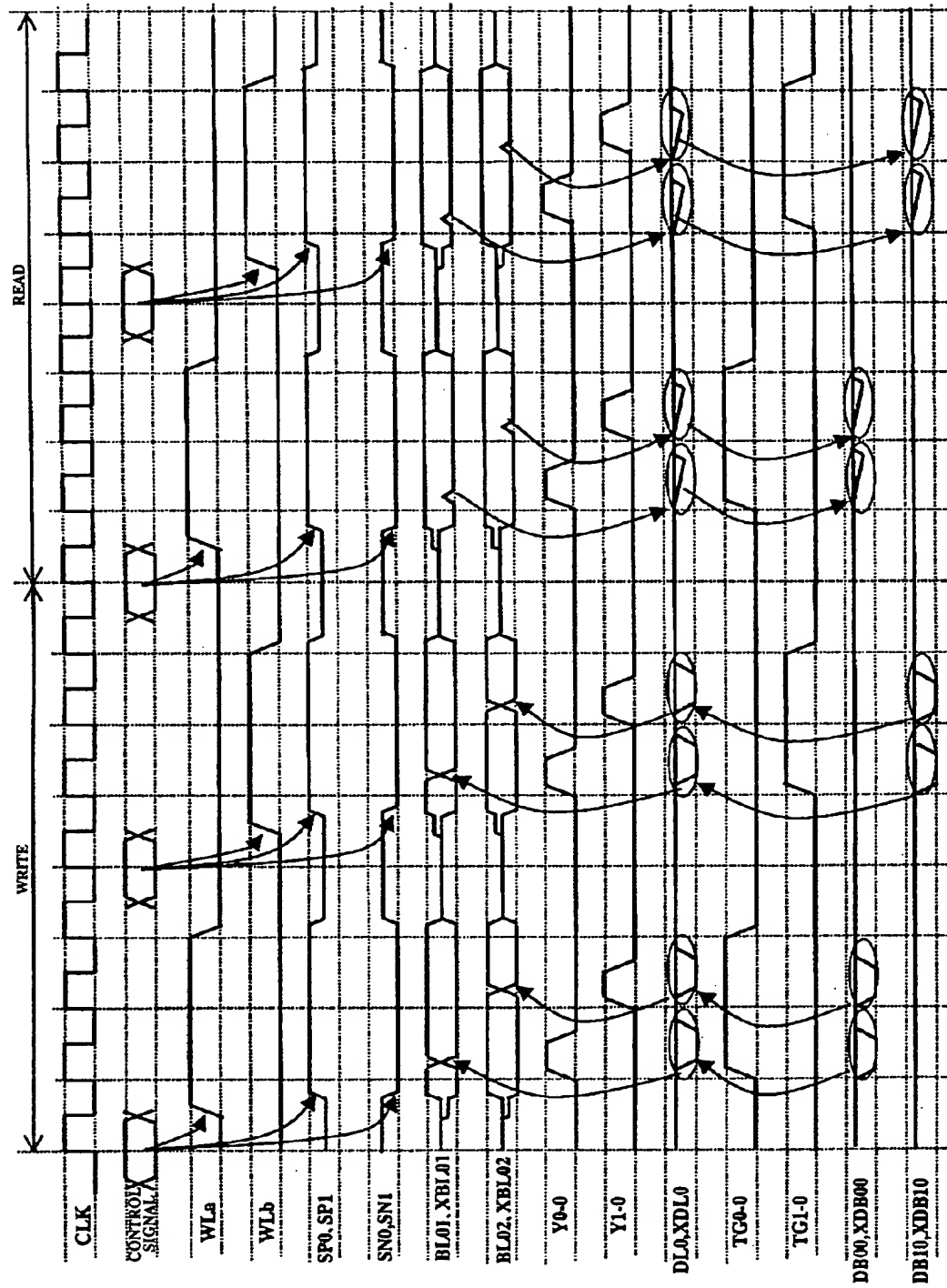


FIG. 4

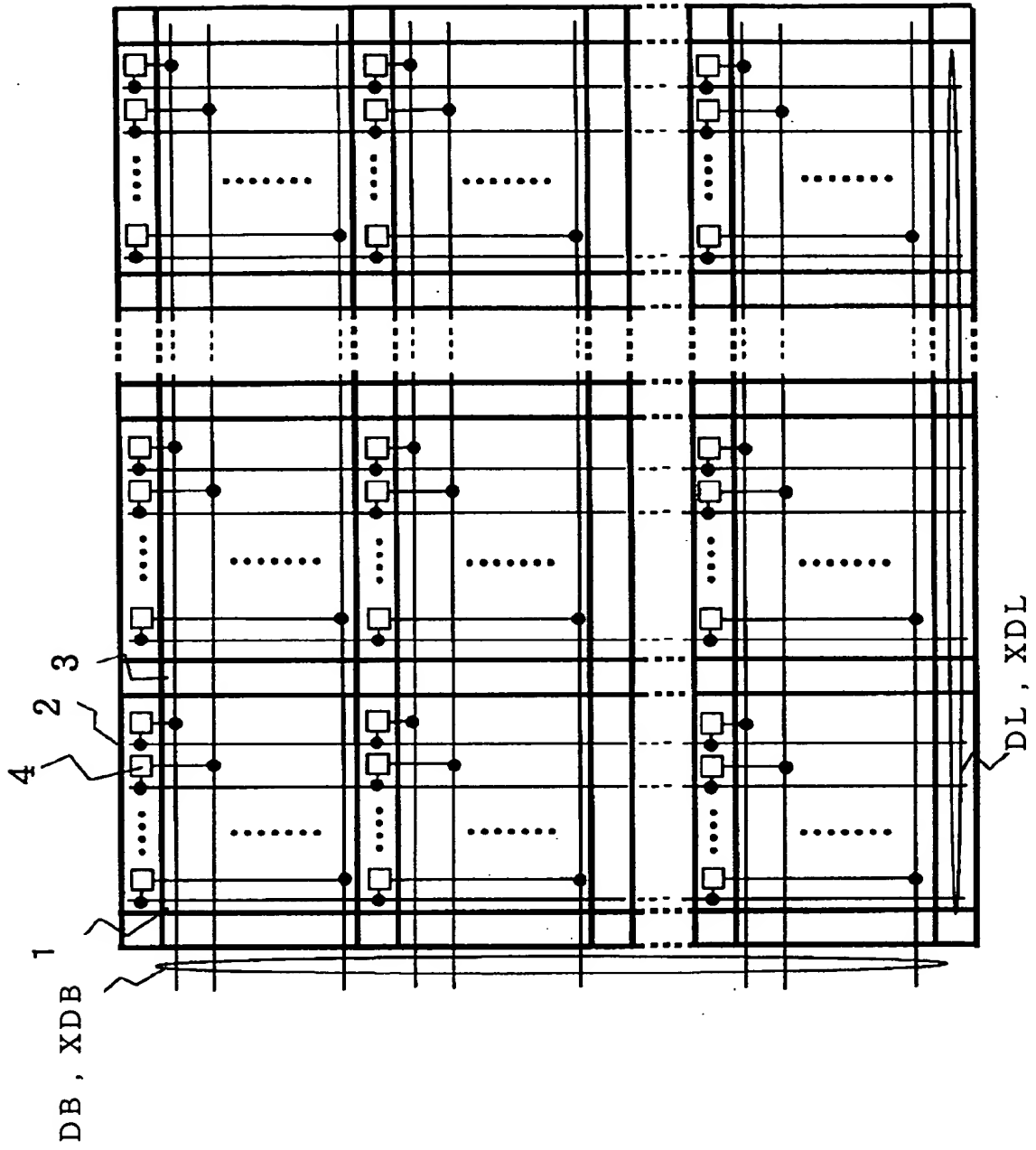






FIG. 7

FIG. 7

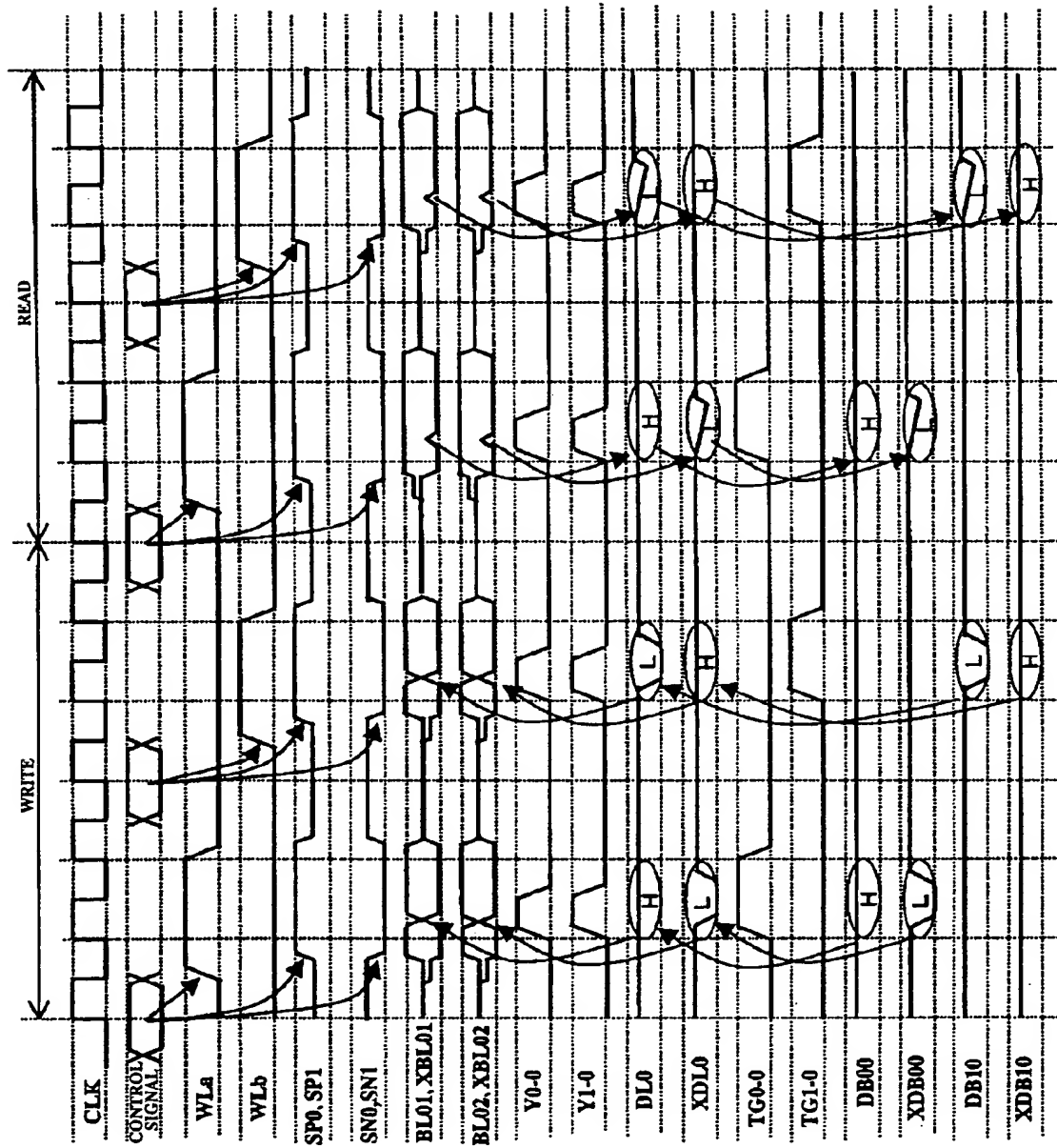
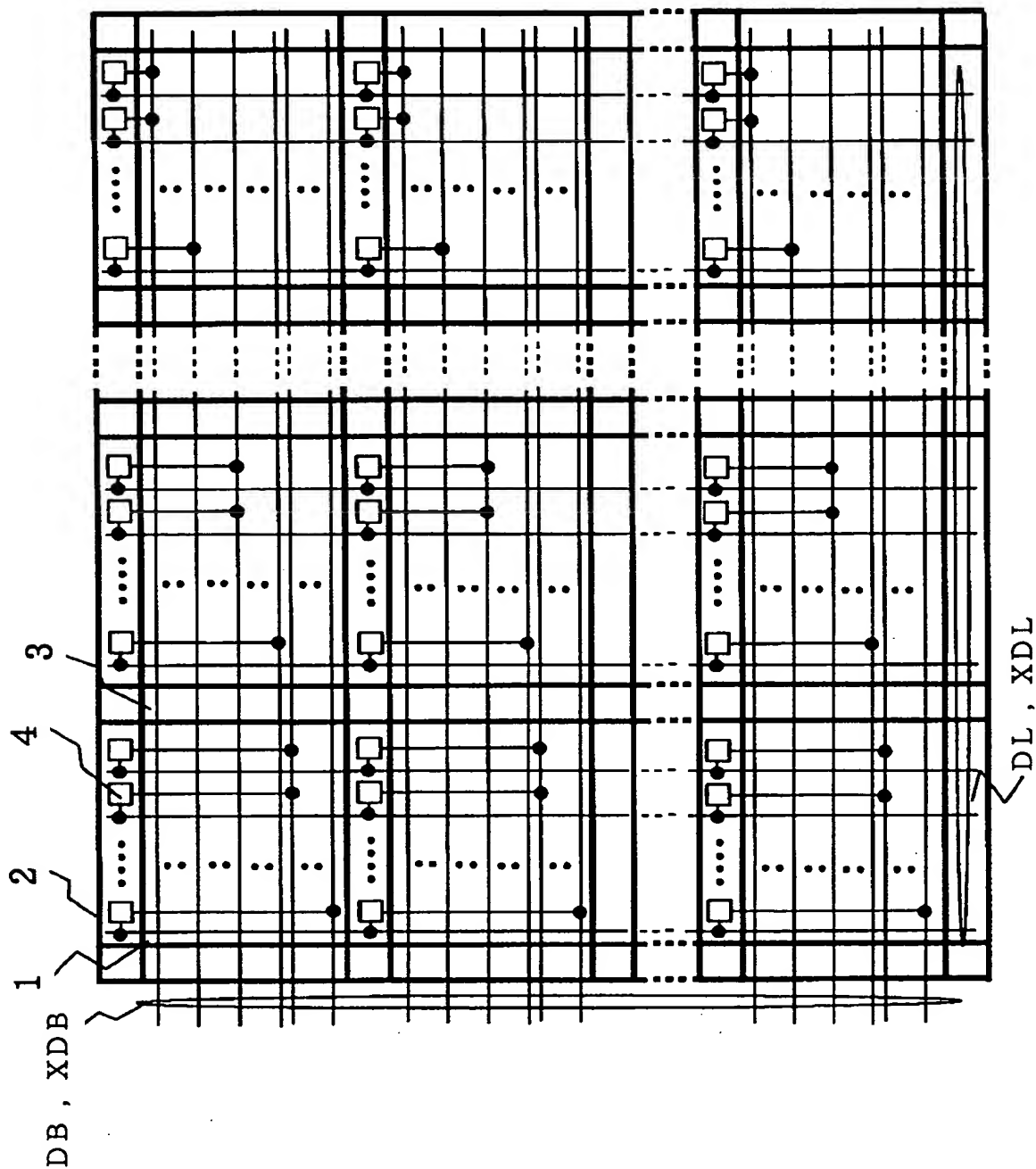


FIG. 8







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FIG. 10

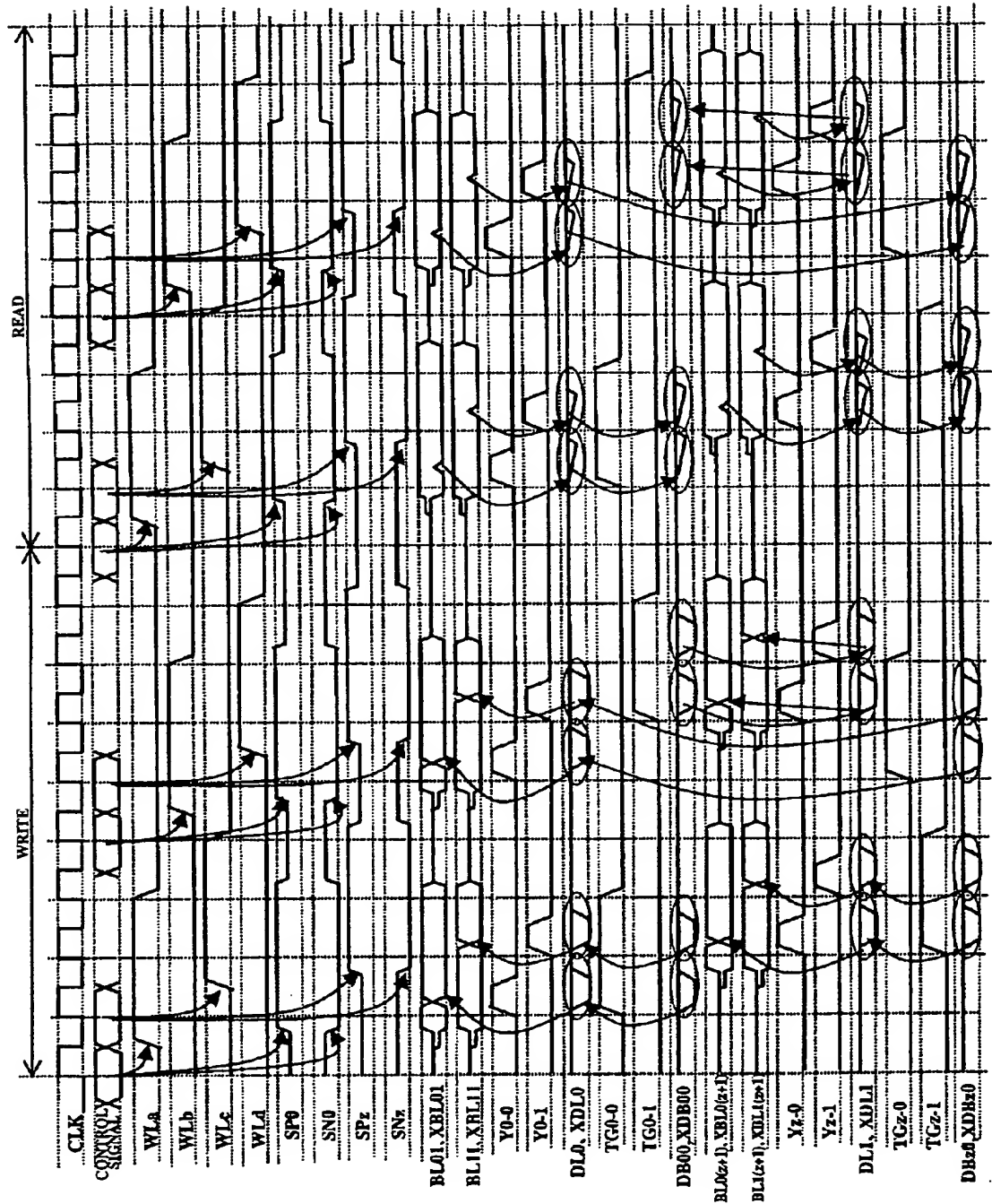


FIG. 11

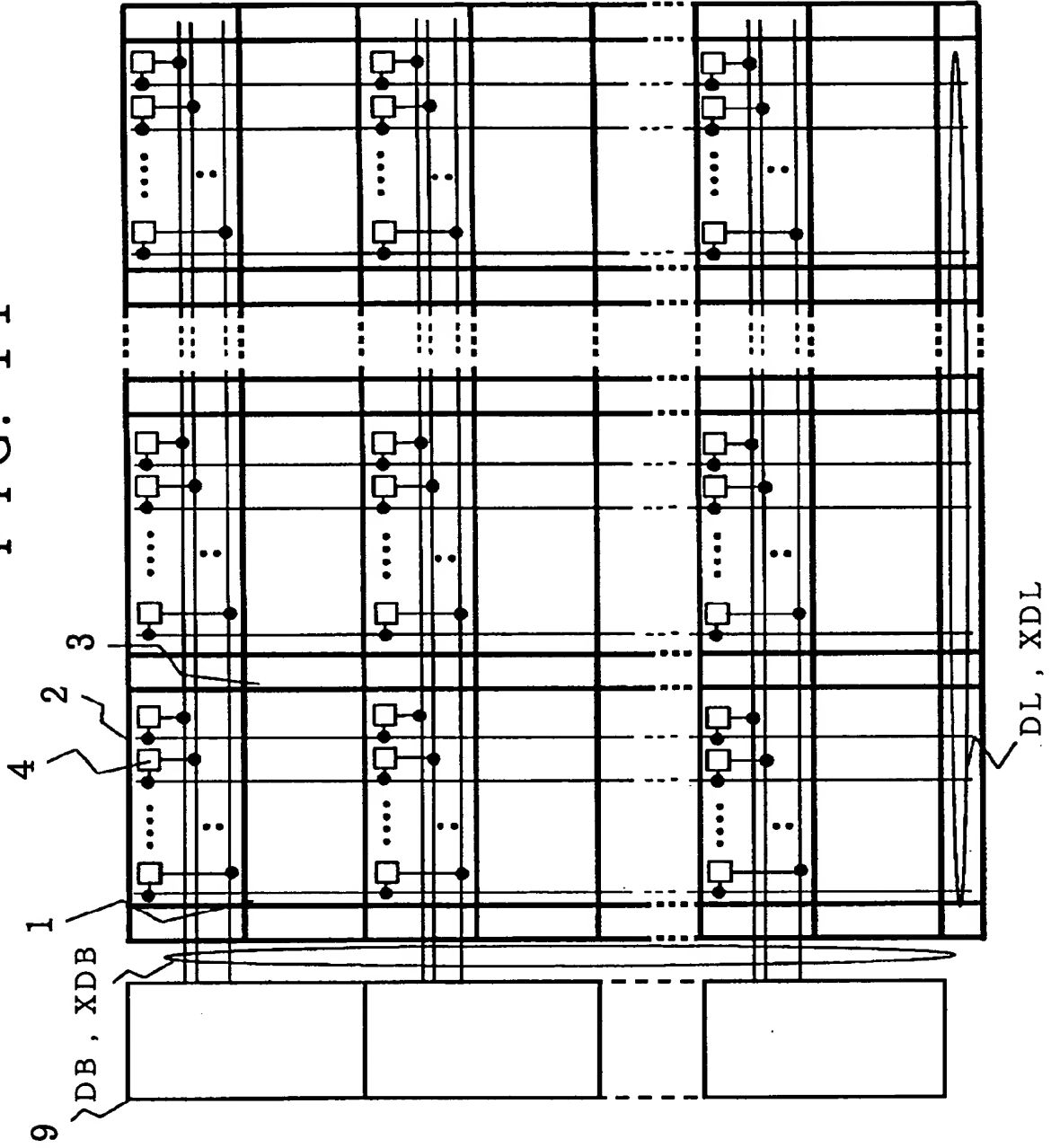


FIG. 12

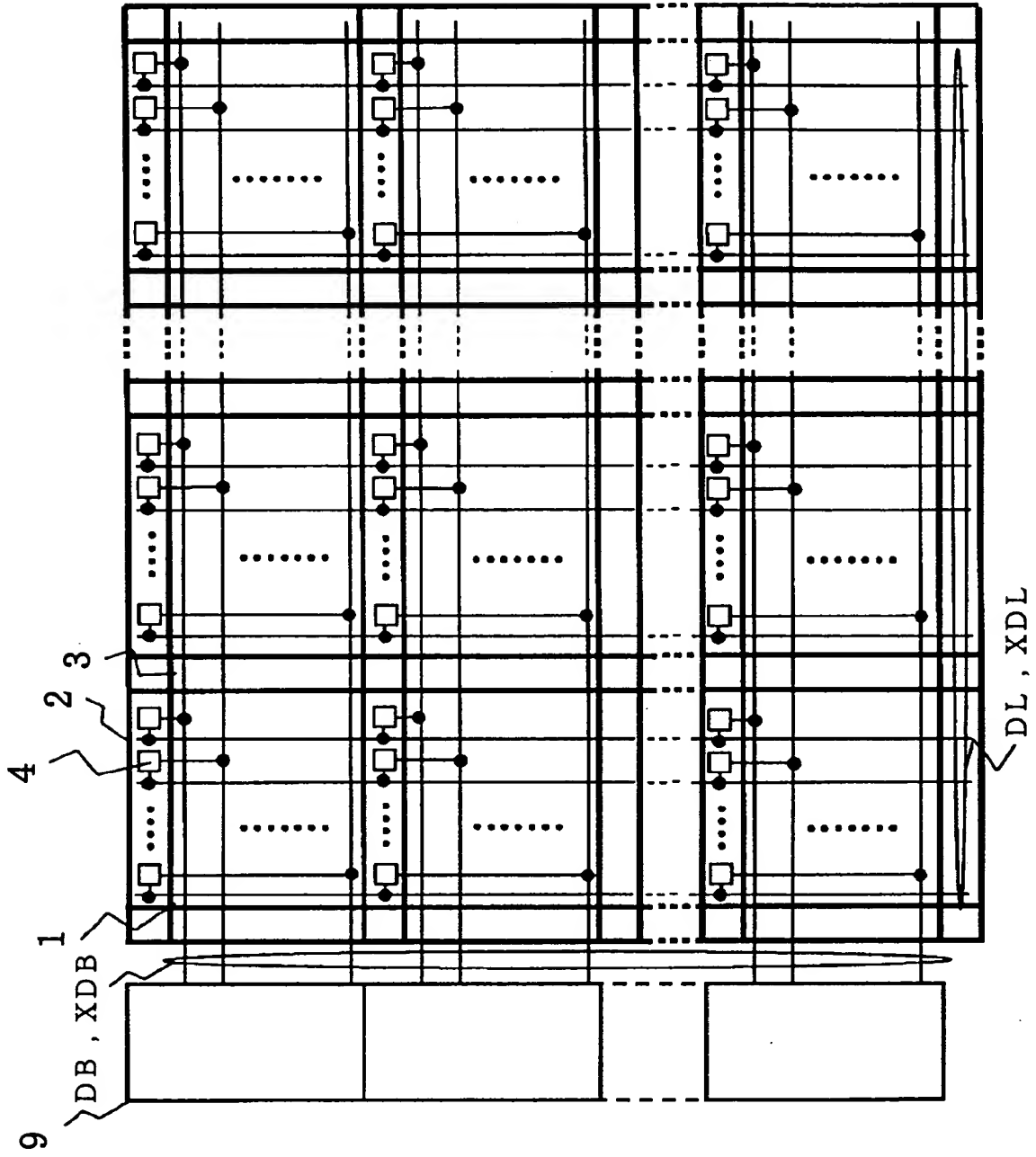


FIG. 13

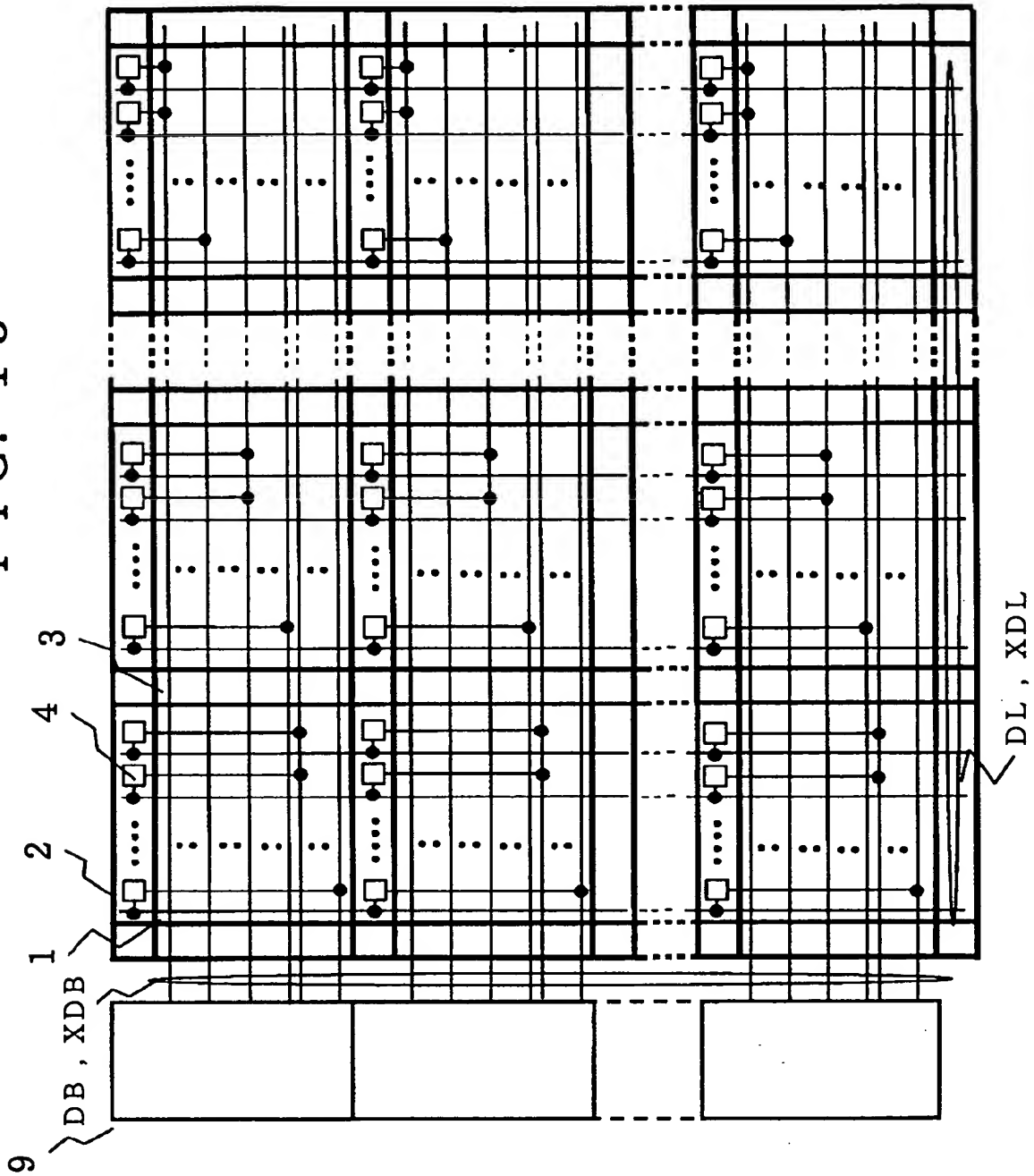


FIG. 14

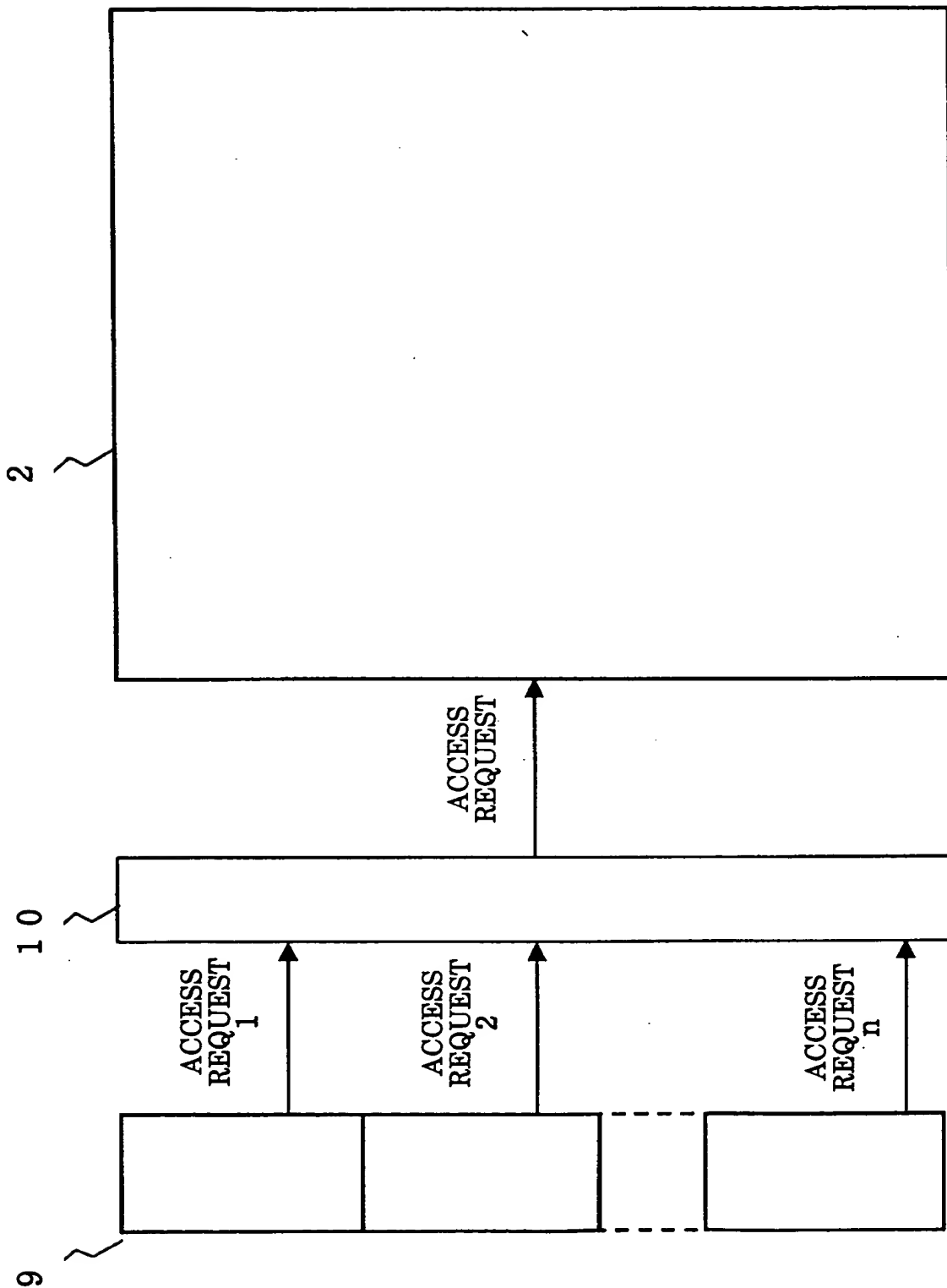


FIG. 15

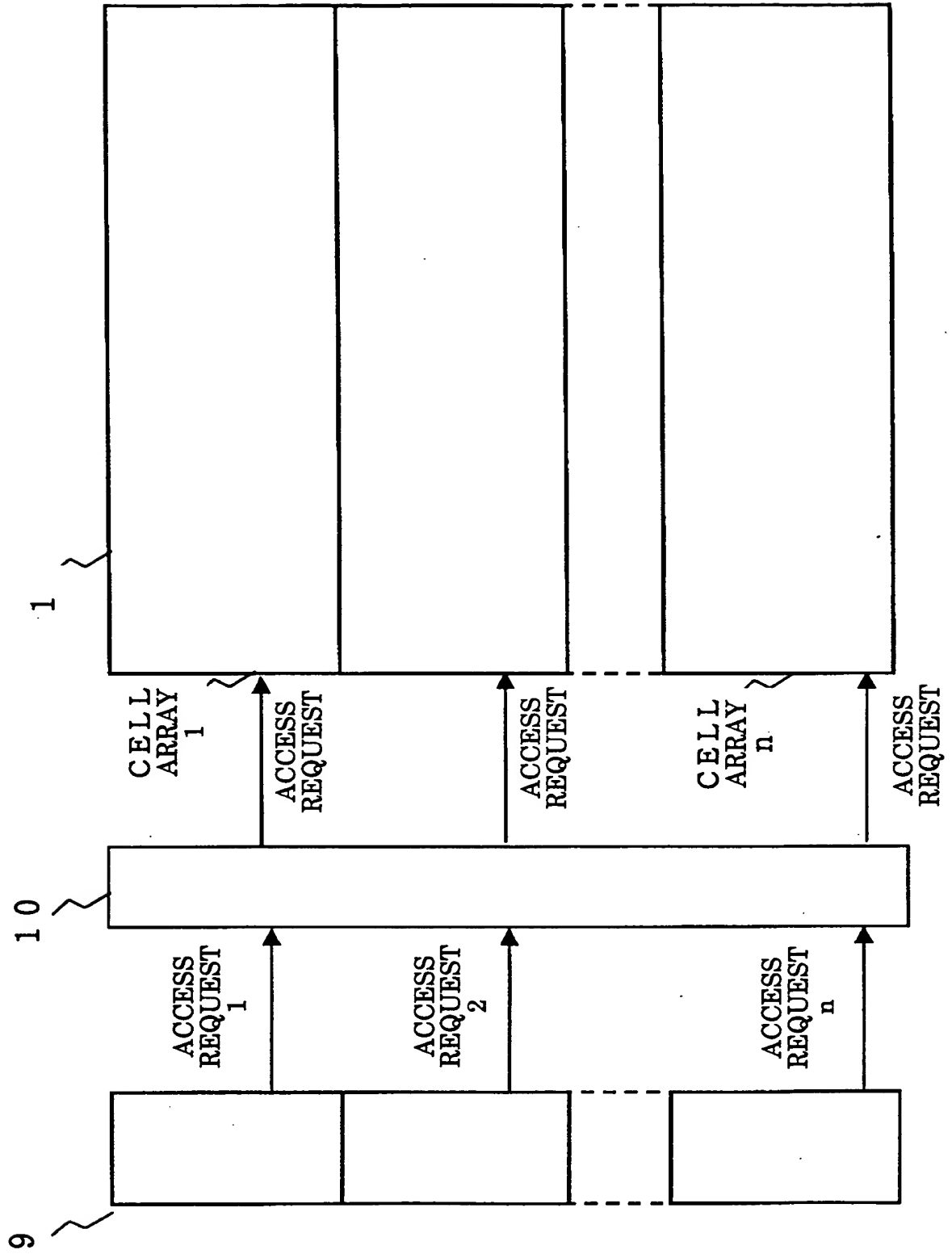
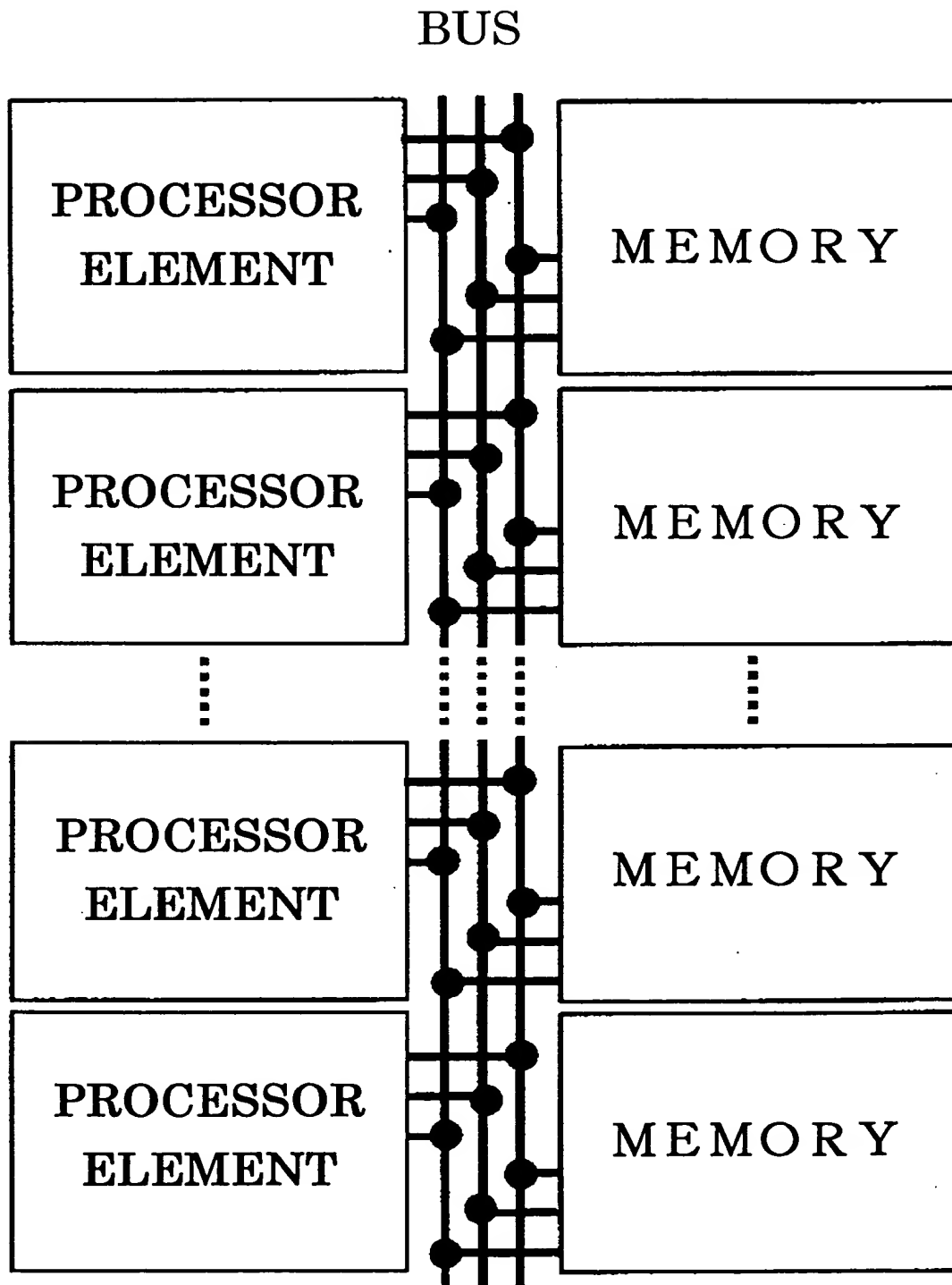


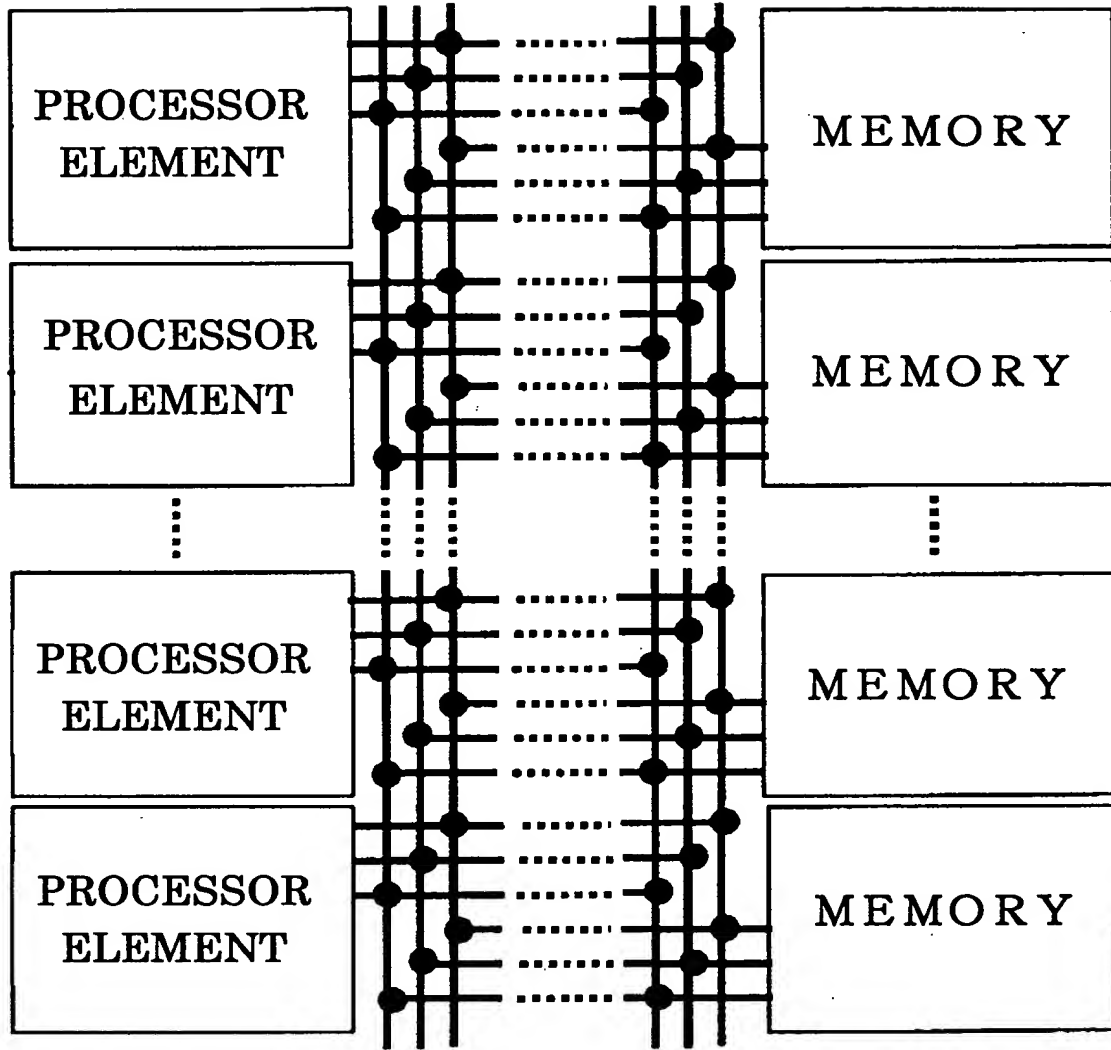
FIG. 16



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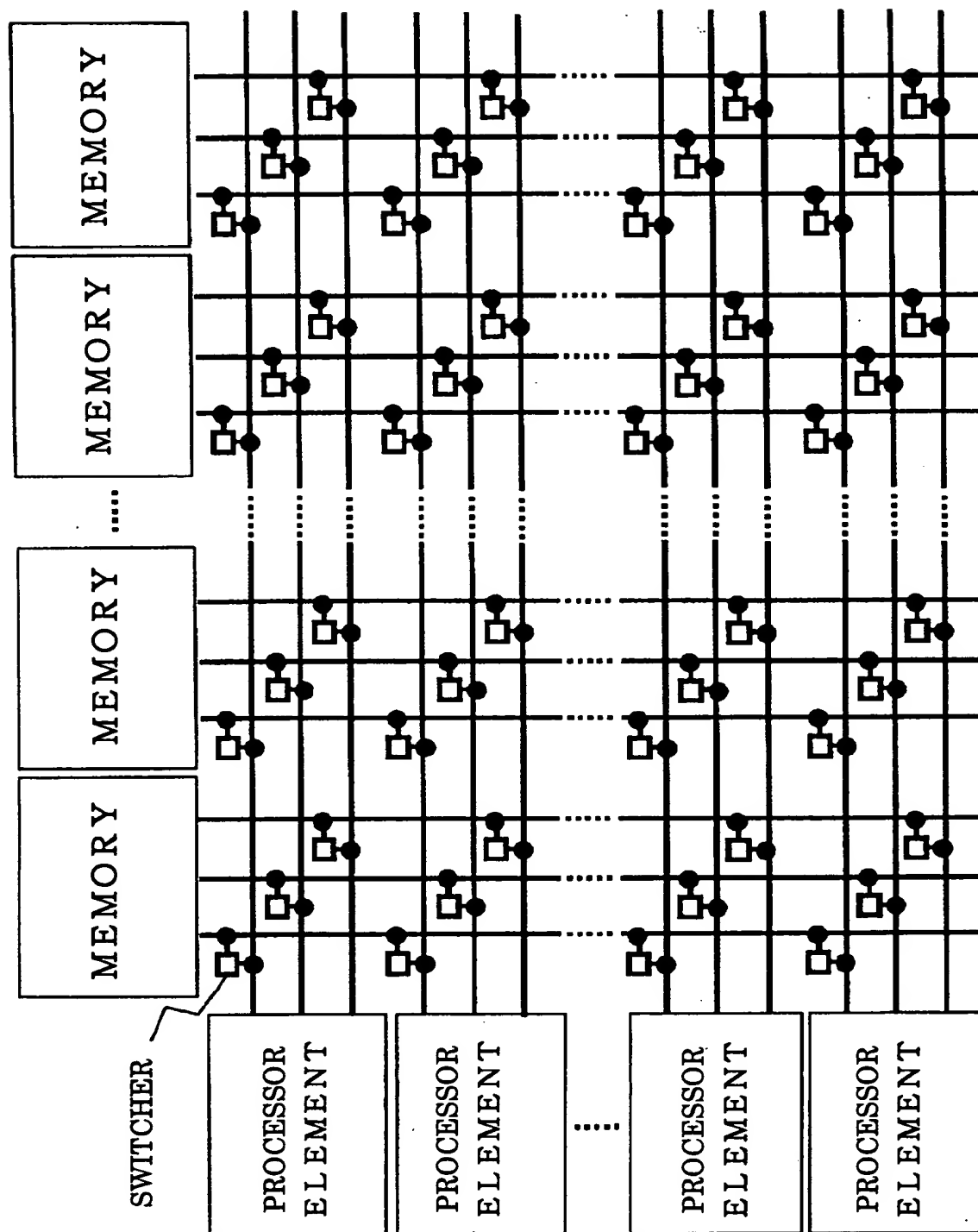


FIG. 17



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FIG. 18



## REFERENCE NUMERALS IN THE DRAWINGS

- 1 CELL ARRAY
- 2 SENSE AMPLIFIER ROW
- 3 SUB-WORD DECODER ARRAY
- 4, 6 SWITCHER
- 5 SENSE AMPLIFIER
- 7 MEMRY CELL
- 8 SELECTION GATE
- 9 PROCESSOR ELEMENT
- 1 0 ARBITER CIRCUIT
- BL,XBL BIT LINE PAIRS
- DL,XDL FIRST DATA LINE PAIRS
- DB,XDB SECOND DATA LINE PAIRS
- Y,TG GATE SIGNAL
- SP,SN SENSE AMPLIFIER STARTING SIGNAL
- WL WORD LINE

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